CLAIMS

1. A method for verification of a system design represented by a model that includes a plurality of variables, the method comprising:

arranging the variables in an Ordered Binary Decision Diagram (OBDD) according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables;

assigning to each processor, among a group of two or more computer processors, a respective variable among the plurality of the variables;

using each processor, reordering the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the processor, until at least one of the processors identifies a new order for the OBDD; and

using the new order of the OBDD, verifying a characteristic of the model against a specification.

2. The method according to claim 1, wherein reordering the rows comprises, using each processor, finding the new order such that the number of the nodes in the OBDD is reduced relative to the initial order.

3. The method according to claim 2, wherein reordering the rows comprises receiving first and second new orders, respectively, from first and second processors among the two or more computer processors, and selecting the new

order from among the first and second new orders so as to minimize the number of the nodes in the OBDD.

4. The method according to claim 1, wherein reordering the rows comprises operating simultaneously with at least two of the processors on a common set of the rows.

5. The method according to claim 4, wherein operating simultaneously comprises operating on substantially all the rows of the OBDD using all of the at least two of the processors.

6. The method according to claim 1, wherein reordering the rows comprises sifting the rows of the OBDD.

7. The method according to claim 1, and comprising replacing the initial order with the new order, and repeating the steps of assigning the respective variable and reordering the rows based on the new order until a predefined reordering criterion is satisfied.

8. The method according to claim 7, wherein the reordering criterion determines a maximum number of the nodes in the BDD.

9. The method according to claim 7, wherein the two or more computer processors comprise first and second processors, and wherein reordering the rows comprises

receiving the new order from the first processor, and wherein replacing the initial order comprises communicating the new order to the second processor for use in repeating the step of reordering the rows.

10. The method according to claim 9, wherein reordering the rows comprises receiving first and second new orders, respectively, from the first and second processors, and selecting the first new order according to a predefined selection criterion.

11. The method according to claim 7, wherein verifying the characteristic comprises operating on the OBDD using the group of computer processors while saving data regarding the OBDD in a memory until a predetermined amount of space in the memory has been consumed, and wherein repeating the steps of assigning the respective variable and reordering the rows comprises repeating the steps after operating on the OBDD to verify the characteristic so as to reduce the amount of space occupied by the OBDD in the memory.

12. The method according to claim 1, wherein verifying the characteristic comprises applying a symbolic model checker to verify the model against the specification.

13. Apparatus for verification of a system design represented by a model that includes a plurality of

variables, the apparatus comprising a master processor and one or more slave processors,

wherein the master processor is arranged to receive an Ordered Binary Decision Diagram (OBDD) representing the model according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables, and to assign to each of the one or more slave processors a respective variable among the plurality of the variables, and

wherein each slave processor is arranged to reorder the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the slave processor, until at least one of the slave processors identifies a new order for the OBDD, and

wherein at least one of the master and slave processors is further arranged to verify a characteristic of the model against a specification using the new order of the OBDD.

14. The apparatus according to claim 13, wherein each of the slave processors is arranged to find the new order such that the number of the nodes in the OBDD is reduced relative to the initial order.

15. The apparatus according to claim 14, wherein the one or more slave processors comprise first and second slave processors, and wherein the master processor is arranged to receive first and second new orders, respectively,

from the first and second slave processors and to select the new order from among the first and second new orders so as to minimize the number of the nodes in the OBDD.

16. The apparatus according to claim 13, wherein the slave processors are arranged so that at least two of the slave processors reorder the rows by operating simultaneously on a common set of the rows.

17. The apparatus according to claim 16, wherein the at least two of the slave processors are arranged to operate simultaneously on substantially all the rows of the OBDD.

18. The apparatus according to claim 13, wherein the slave processors are arranged to reorder the rows by sifting the rows of the OBDD.

19. The apparatus according to claim 13, wherein the master processor is arranged to replace the initial order with the new order, and repeat assigning a new respective variable to each of the one or more slave processors, so as to cause the slave processors to repeat reordering the rows based on the new order until a predefined reordering criterion is satisfied.

20. The apparatus according to claim 19, wherein the reordering criterion determines a maximum number of the nodes in the BDD.

21. The apparatus according to claim 19, wherein the one or more slave processors comprise first and second slave processors, and wherein the master processor is arranged to receive the new order from the first processor, and to communicate the new order to the second processor for use in repeating the reordering of the rows.

22. The apparatus according to claim 21, wherein the master processor is arranged to receive first and second new orders, respectively, from the first and second slave processors, and to select the first new order according to a predefined selection criterion.

23. The apparatus according to claim 19, and comprising a memory, wherein the at least one of the master and slave processors is arranged to verify the characteristic of the model by operating on the OBDD while saving data regarding the OBDD in the memory until a predetermined amount of space in the memory has been consumed, and

wherein the master processor is arranged to assign the new respective variable to each of the slave processors and to cause the slave processors to repeat the reordering of the rows so as to reduce the amount of space occupied by the OBDD in the memory due to operating on the OBDD to verify the characteristic.

24. The apparatus according to claim 13, wherein the at least one of the master and slave processors is arranged

to apply a symbolic model checking program in order to verify the model against the specification.

25. The apparatus according to claim 13, wherein the master processor is further arranged to function as one of the slave processors.

26. A computer software product for verification of a system design represented by a model that includes a plurality of variables, the product comprising a computer-readable medium in which program instructions are stored, which instructions, when read by a group of two or more computer processors in mutual communication, cause one of the computer processors to serve as a master processor, and cause one or more of the computer processors to serve as slave processors,

wherein the instructions cause the master processor to receive an Ordered Binary Decision Diagram (OBDD) representing the model according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables, and to assign to each of the one or more slave processors a respective variable among the plurality of the variables, and

wherein the instructions cause each slave processor to reorder the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the slave processor, until at least one of the slave processors identifies a new order for the OBDD, and

wherein the instructions further cause at least one of the computer processors to verify a characteristic of the model against a specification using the new order of the OBDD.

27. The product according to claim 26, wherein the instructions cause each of the slave processors to find the new order such that the number of the nodes in the OBDD is reduced relative to the initial order.

28. The product according to claim 27, wherein the instructions cause at least two of the computer processors to serve respectively as first and second slave processors, and wherein the instructions cause the master processor to receive first and second new orders, respectively, from the first and second slave processors and to select the new order from among the first and second new orders so as to minimize the number of the nodes in the OBDD.

29. The product according to claim 26, wherein the instructions cause at least two of the computer processors to serve as slave processors, and further cause the at least two of the processors to reorder the rows by operating simultaneously on a common set of the rows.

30. The product according to claim 29, wherein the instructions cause the at least two of the processors to

operate simultaneously on substantially all the rows of the OBDD.

31. The product according to claim 26, wherein the instructions cause the slave processors to reorder the rows by sifting the rows of the OBDD.

32. The product according to claim 26, wherein the instructions cause the master processor to replace the initial order with the new order, and to repeat assigning a new respective variable to each of the slave processors, so as to cause the slave processors to repeat reordering the rows based on the new order until a predefined reordering criterion is satisfied.

33. The product according to claim 32, wherein the reordering criterion determines a maximum number of the nodes in the BDD.

34. The product according to claim 32, wherein the instructions cause at least two of the computer processors to serve respectively as first and second slave processors, and wherein the instructions cause the master processor to receive the new order from the first processor, and to communicate the new order to the second processor for use in repeating the reordering of the rows.

35. The product according to claim 34, wherein the instructions cause the master processor to receive first and second new orders, respectively, from the first and second slave processors, and to select the first new order according to a predefined selection criterion.

36. The product according to claim 32, wherein the instructions cause the at least one of the computer processors to verify the characteristic of the model by operating on the OBDD while saving data regarding the OBDD in a memory until a predetermined amount of space in the memory has been consumed, and

wherein the instructions further cause the master processor to assign the new respective variable to each of the slave processors and to cause the slave processors to repeat the reordering of the rows so as to reduce the amount of space occupied by the OBDD in the memory due to operating on the OBDD to verify the characteristic.

37. The product according to claim 26, wherein the instructions cause the at least one of the computer processors is arranged to apply a symbolic model checking program in order to verify the model against the specification.

38. The product according to claim 26, wherein the instructions further cause the master processor to function as one of the slave processors.

39. A method for modeling a target system, the method comprising:

identifying a plurality of variables that characterize the target system and a Boolean function that is applicable to the variables;

responsively to the Boolean function, arranging the variables in an Ordered Binary Decision Diagram (OBDD) according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables;

assigning to each processor, among a group of two or more computer processors, a respective variable among the plurality of the variables; and

using each processor, reordering the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the processor, until at least one of the processors identifies a new order for the OBDD.

40. The method according to claim 39, wherein reordering the rows comprises operating simultaneously with at least two of the processors on a common set of the rows.

41. The method according to claim 40, wherein operating simultaneously comprises operating on substantially all the rows of the OBDD using all of the at least two of the processors.

42. The method according to claim 39, and comprising replacing the initial order with the new order, and repeating the steps of assigning the respective variable and reordering the rows based on the new order until a predefined reordering criterion is satisfied.

43. The method according to claim 42, wherein the two or more computer processors comprise first and second processors, and wherein reordering the rows comprises receiving the new order from the first processor, and wherein replacing the initial order comprises communicating the new order to the second processor for use in repeating the step of reordering the rows.

44. Apparatus for modeling a target system, comprising a master processor and one or more slave processors,

wherein the master processor is arranged to receive a model of the target system characterized by a plurality of variables and a Boolean function, wherein the model is represented by an Ordered Binary Decision Diagram (OBDD) according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables, and

wherein the master processor is arranged to assign to each of the one or more slave processors a respective variable among the plurality of the variables, and

wherein each slave processor is arranged to reorder the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective

variable that is assigned to the slave processor, until at least one of the slave processors identifies a new order for the OBDD.

45. The apparatus according to claim 44, wherein the slave processors are arranged so that at least two of the slave processors reorder the rows by operating simultaneously on a common set of the rows.

46. The apparatus according to claim 45, wherein the at least two of the slave processors are arranged to operate simultaneously on substantially all the rows of the OBDD.

47. The apparatus according to claim 44, wherein the master processor is arranged to replace the initial order with the new order, and repeat assigning a new respective variable to each of the one or more slave processors, so as to cause the slave processors to repeat reordering the rows based on the new order until a predefined reordering criterion is satisfied.

48. The apparatus according to claim 47, wherein the one or more slave processors comprise first and second slave processors, and wherein the master processor is arranged to receive the new order from the first processor, and to communicate the new order to the second processor for use in repeating the reordering of the rows.

49. The apparatus according to claim 44, wherein the master processor is further arranged to function as one of the slave processors.

50. A computer software product for modeling a target system, the product comprising a computer-readable medium in which program instructions are stored, which instructions, when read by a group of two or more computer processors in mutual communication, cause one of the computer processors to serve as a master processor, and cause one or more of the computer processors to serve as slave processors,

wherein the instructions cause the master processor to receive a model of the target system characterized by a plurality of variables and a Boolean function, wherein the model is represented by an Ordered Binary Decision Diagram (OBDD) according to an initial order of the variables, the OBDD comprising a number of nodes arranged in rows corresponding respectively to the plurality of the variables, and

wherein the instructions further cause the master processor to assign to each of the one or more slave processors a respective variable among the plurality of the variables, and

wherein the instructions cause each slave processor to reorder the rows of the OBDD by varying a position in the OBDD of one of the rows, which corresponds to the respective variable that is assigned to the slave processor, until at least one of the slave processors identifies a new order for the OBDD, and

wherein the instructions further cause at least one of the computer processors to verify a characteristic of the model against a specification using the new order of the OBDD.

51. The product according to claim 50, wherein the instructions cause at least two of the computer processors to serve as slave processors, and further cause the at least two of the processors to reorder the rows by operating simultaneously on a common set of the rows.

52. The product according to claim 51, wherein the instructions cause the at least two of the processors to operate simultaneously on substantially all the rows of the OBDD.

53. The product according to claim 50, wherein the instructions cause the master processor to replace the initial order with the new order, and to repeat assigning a new respective variable to each of the slave processors, so as to cause the slave processors to repeat reordering the rows based on the new order until a predefined reordering criterion is satisfied.

54. The product according to claim 53, wherein the instructions cause at least two of the computer processors to serve respectively as first and second slave processors, and wherein the instructions cause the

master processor to receive the new order from the first processor, and to communicate the new order to the second processor for use in repeating the reordering of the rows.